COMPUTER PROCESSOR READ/ALTER/REWRITE OPTIMIZATION CACHE INVALIDATE SIGNALS

Abstract of the Disclosure

A plurality of processors in a data processing system share a common memory through which they communicate and share resources. When sharing resources, one processor needs to wait for another processor to modify a specified location in memory, such as unlocking a lock. Memory and bus traffic are minimized during this waiting by first reading and testing the memory location. Then, the memory location is not read and tested again until the local copy of the cache line containing that memory location is invalidated by another processor. This feature is utilized both for a Lock instruction and a Wait for Change instruction, both of which utilize a timer parameter for specifying a maximum number of cycles to wait for another processor to modify the specified location in memory.